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10EC/TE61

Sixth Semester B.E. Degree Examination, June/July 2019

Digital Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Compare analog and digital communication. **(04 Marks)**

b. Derive the interpolation formula for reconstructing the original signal from the sequence of sampled values. **(08 Marks)**

c. The signal $x(t) = 12\cos(800\pi t)\cos^2 1800\pi t$ is ideally sampled at 4600 samples/sec. What is the minimum allowable sampling frequency? What is the range of the cut-off frequency for the lowpass filter? Draw the frequency components present in the output of the lowpass filter. **(08 Marks)**

2 a. Derive an expression for output SNR of the quantizer and show that $(SNR)_0 = 1.76 + 6n$ in db if a sinusoidal signal is quantized. **(08 Marks)**

b. What is the need for non-uniform quantization? Explain μ-law and A-law compounding. **(08 Marks)**

c. A PCM system uses a uniform quantizer followed by a 7 bit binary encoder. The bit rate of the system is equal to 50×10^6 bits/sec:
i) What is the sampling frequency?
ii) Calculate the $(SNR)_0$. **(04 Marks)**

3 a. What is slope overload distortion and granular noise in delta modulation and how can it be reduced? **(08 Marks)**

b. Obtain the expression for power spectral density of NRZ unipolar format. **(06 Marks)**

c. Explain T1 carrier system. **(06 Marks)**

4 a. Explain ISI. Derive an expression for Nyquist pulse shaping criterion for distortionless baseband binary transmission. **(08 Marks)**

b. Explain eye pattern. **(06 Marks)**

c. A continuous time signal is connected into a PCM wave. The number of quantization levels = 64. A synchronizing pulse is added at the end of each code word representing a sample of the analog signal. The resulting PCM is sent over a channel of bandwidth 24 kHz using a binary PAM system with raised cosine spectrum with roll of = 1.
i) Find the bit rate
ii) Find the sampling rate
iii) What is the highest frequency of the continuous time signal? **(06 Marks)**

PART – B

5 a. With a block diagram, explain coherent QPSK transmitter and receiver. **(08 Marks)**

b. Explain non-coherent DPSK system. **(06 Marks)**

c. For a given binary sequence 01101000 sketch the inphase and quadrature phase components of QPSK. Adding these two get the final waveform. **(06 Marks)**

6 a. Explain the two stage Gram-Schmidt orthogonalization procedure to find the orthonormal functions. **(10 Marks)**

b. Derive the equation for maximum likelihood estimation. **(10 Marks)**

7 a. List the properties of a matched filter receiver. **(08 Marks)**

b. Show that the probability of bit error of a matched filler receiver is given by $P_e = \frac{1}{2}\operatorname{erfc}\sqrt{\frac{E_b}{N_o}}$. **(08 Marks)**

c. Let s(t) be a rectangular pulse of amplitude A and duration T seconds, applied to the input of a filter matched to s(t). Determine the output signal to noise ratio of the filter at t = T in terms of noise power spectral density. **(04 Marks)**

8 a. What is spread spectrum? Explain the principle of direct sequence spread spectrum system. **(08 Marks)**

b. Explain the properties of PN sequence. **(06 Marks)**

c. In a DSSS it is required to have a jamming margin greater than 26 dB. The ratio E_b/N_o is set at 10. Determine the minimum processing gain and the minimum number of stages required to generate the maximum length of sequence. **(06 Marks)**

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10EC/TE62

Sixth Semester B.E. Degree Examination, June/July 2019
Microprocessors

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. With necessary diagram explain programming model of 8086 microprocessor. **(10 Marks)**

b. Explain 2nd byte of 8086 instruction template. Also find machine code for ADC [BX + 06], AL. Given opcode of ADC is "000100". **(10 Marks)**

2 a. Indicate whether the following instructions are valid or not. If your answer is "not valid" then explain why?
i) MOV AL, BX
ii) MOV AL, [BX]
iii) XLAT CX
iv) RCR DH, 06H **(08 Marks)**

b. Given, CS = 4000H, DS = 20A0H BX = 1200H, SI = 06BCH, DI = 1ABCH, disp = 4AH. Obtain physical address for,
i) MOV CL, [SI + DI + disp]
ii) MOV AX, [BX]
iii) ADD BL, [BX + SI] **(06 Marks)**

c. Explain the tools used for implementation of assembly language programming. **(06 Marks)**

3 a. Without using dummy memory block write an ALP to perform reverse block transfer of 20 memory bytes stored in consecutive locations starting from LOC. **(08 Marks)**

b. Explain REP prefixes available in 8086. **(04 Marks)**

c. Using recursive procedure write an ALP to find factorial of an 8-bit number read from keyboard. **(08 Marks)**

4 a. WALP to replace a character by given character in the string stored in memory location starting from MEM. **(06 Marks)**

b. Explain the dedicated interrupts available in 8086 μP. **(10 Marks)**

c. Using suitable example explain how the microprocessor finds the address of an ISS for particular interrupt. **(04 Marks)**

PART – B

5 a. Compare memory mapped I/O and I/O mapped IO interfacing schemes. **(04 Marks)**

b. What do you mean by key debouncing? Show how a 4 × 4 matrix keyboard can be interfaced to 8086 μP. Also WALP to read a key from it. (Include S/W key debounce logic). **(10 Marks)**

c. WALP to rotate the stepper for 720° in clockwise direction. **(06 Marks)**

6 a. What do you mean by coprocessor? Explain the features of 8087 NDP. (08 Marks)
b. Represent $(3.625)_{10}$ into its short real format. (04 Marks)
c. Differentiate between:
i) Forward and reverse division
ii) FADD and FADDP
iii) FSTSW and FNSTSW
iv) FTST and FXAM (08 Marks)

7 a. Explain following terms with respect to 8086 μP:
i) ALE ii) $AD_0 - AD_{15}$ iii) $DT/\overline{R}$ iv) $MN/\overline{MX}$ v) $\overline{LOCK}$ (10 Marks)
b. Write a note on signals used for parallel printer interface. (08 Marks)
c. What do you mean by pipelining? (02 Marks)

8 a. Explain modes of operations of 80386 processor. (08 Marks)
b. Explain additional features of Pentium in comparison to 80386 processor. (10 Marks)
c. Define cache hit rate. (02 Marks)

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10EC63

Sixth Semester B.E. Degree Examination, June/July 2019
Microelectronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any THREE full questions from Part-A and any TWO full questions from Part-B.***

PART – A

1 a. With a diagram and characteristic curves, derive relationship between $i_D - V_{DS}$ and discuss the characteristics for an enhancement NMOS transistor. **(10 Marks)**

b. Analyze the circuit shown in Fig.Q.1(b) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1V$, $K_n^1\left(\frac{W}{L}\right) = 1mA/V^2$ and assume $\lambda = 0$. **(05 Marks)**

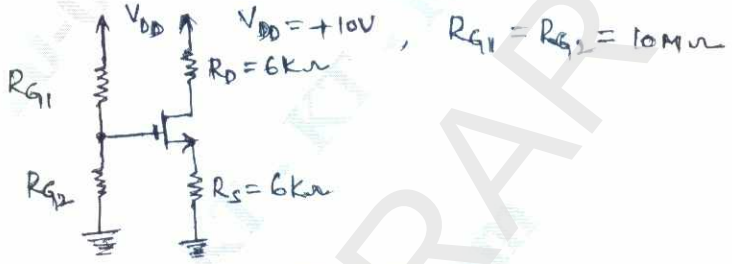

Fig.Q.1(b)

c. Consider a process technology for which $L_{min} = 0.4\mu m$, $t_{ox} = 8nm$, $\mu_n = 450\ cm^2/v.s$ and $V_t = 0.7v$,

i) Find C_{ox} and k_n^1

ii) For a MOSFET with W/L = 8μm/0.8μm, calculate the values of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100\mu A$.

iii) For the device in (ii), find the value of V_{GS} required to cause the device to operate as a 1000Ω resistor for very small V_{DS}. **(05 Marks)**

2 a. Explain the following with the help of a diagram and waveforms:

i) DC bias point

ii) Signal current in the drain terminal

iii) Voltage gain. Derive appropriate equations. **(10 Marks)**

b. For the devices in the circuit of Fig.Q.2(b), $|V_t| = 1v$, $\lambda = 0$, $\gamma = 0$, $\mu_n C_{ox} = 50\mu A/v^2$, L = 1μm, w = 10μm, find V_2 and I_2. How do these values change if Q_3 and Q_4 are made to have W = 100μm? **(05 Marks)**

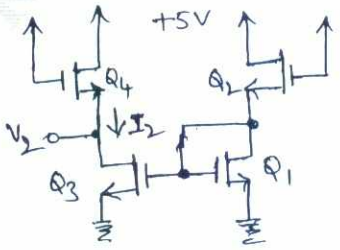

Fig.Q.2(b)

c. Using the feedback bias arrangement shown in Fig.Q.2(c) with a, 9V supply and NMOS device for which V_t = 1v, $K_n^1\left(\frac{W}{L}\right) = 0.4mA/v^2$, find R_D to establish a drain current of 0.2mA. If resistor values are limited to those on the 5% resistor scale, what value would you choose? What values of current and V_D result? **(05 Marks)**

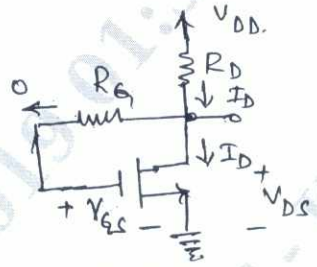

Fig.Q.2(c)

3 a. Discuss the IC biasing techniques with relevant diagrams and expressions. **(10 Marks)**

b. Fig.Q.3(b) shows the high-frequency equivalent circuit of a common source MOSFET amplifier. For R_{sig} = 100KΩ, R_{in} = 420KΩ, $C_{gs} = C_{gd}$ = 1pf, g_m = 4mA/v, R_L^1 = 3.33KΩ, find the mid band voltage gain A_m and the upper 3-dB frequency, f_H. **(06 Marks)**

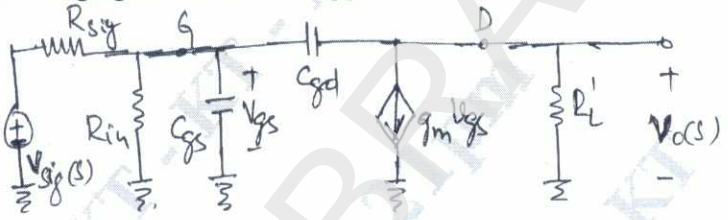

Fig.Q.3(b)

c. With an equivalent circuit discuss Miller's theorem. **(04 Marks)**

4 a. A CMOS common-source amplifier shown in Fig.Q.4(a) has W/L = 7.2 μm/0.36μm for all transistors, $\mu_n C_{ox}$ = 387 μA/v², $\mu_p C_{ox}$ = 86 μA/v², I_{REF} = 100μA, $V_{An}^1 = 5v/\mu m$, $|V_{AP}^1| = 6V/\mu m$. For Q_1, C_{gs} = 20fF, C_{gd} = 5fF, C_L = 25fF, R_{sig} = 10KΩ. Assume C_L includes all capacitances of Q_2 at the output mode. Find f_H using Miller equivalence and the open circuit time constants. Also determine the exact values of fp_1, fp_2 and fz and hence provide another estimate for f_H. **(09 Marks)**

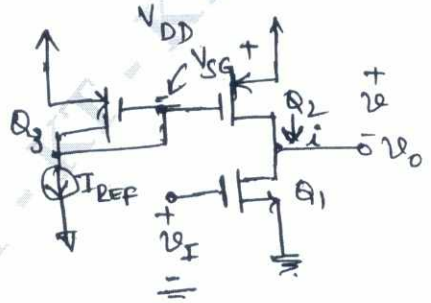

Fig.Q.4(a)

b. Derive an expression for voltage gain and high frequency response of CG amplifier with active loads. **(08 Marks)**

c. Discuss the bipolar mirror with base-current compensation. **(03 Marks)**

5 a. With diagram, derive an expression for input offset voltage of the differential pair. **(07 Marks)**

b. Consider an active-loaded MOS differential amplifier shown in Fig.Q.5(b). Assume for all transistors, $\frac{W}{L} = 8.2\mu m / 0.36\mu m$, $C_{gs} = 20fF$, $C_{gd} = 5fF$, $C_{db} = 5\ fF$. Let $\mu_n C_{ox} = 387\ \mu A/v^2$, $\mu_p C_{ox} = 86\ \mu A/v^2$, $V'_{An} = 5v/\mu m$, $|V'_{Ap}| = 6v/\mu m$. Bias current I = 0.2mA, $R_{ss} = 25K\Omega$, $C_{ss} = 0.2PF$ and the capacitance at output node $C_x = 25fF$. Determine the low-frequency values of A_d, A_{cm} and CMRR. Also find the poles and zero of A_d and the dominant pole of CMRR. **(09 Marks)**

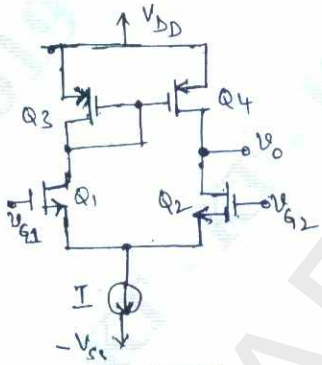

Fig.Q.5(b)

c. With a diagram, explain the two-stage CMOS OPAmp. **(04 Marks)**

PART – B

6 a. Explain the properties of negative feedback. **(08 Marks)**

b. For the OpAmp circuit shown in Fig.Q.6(b), $\mu = 10^4$, $R_{id} = 100K\Omega$, $r_0 = 1k\Omega$, $R_L = 2K\Omega$, $R_1 = 1K\Omega$, $R_2 = 1M\Omega$ and $R_s = 10K\Omega$. Find the values for A, β, the closed – loop gain (v_o/v_s), input resistance (R_{in}) and the output resistance (R_{out}). **(07 Marks)**

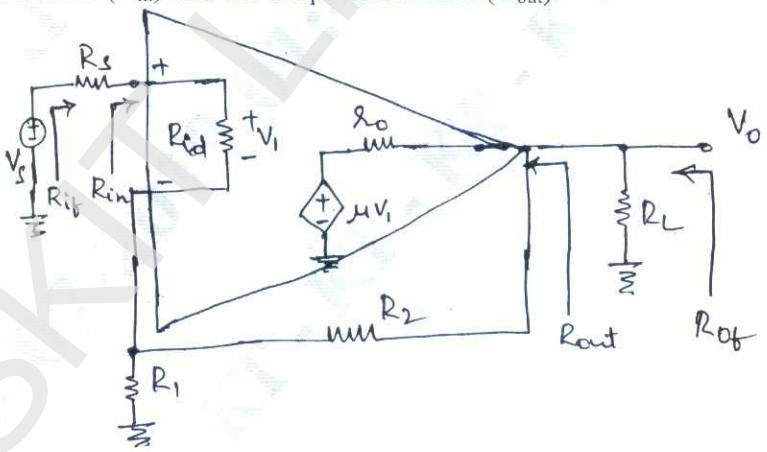

Fig.Q.6(b)

c. Discuss the effect of feedback on the amplifier with two-pole response. **(05 Marks)**

7 a. Discuss and derive an expression for output voltage of antilogarithmic amplifiers. **(05 Marks)**

b. With a diagram, derive an expression for common mode gain of single Op-Amp difference amplifier. **(07 Marks)**

c. Assuming OpAmp to be ideal, derive an expression for closed-loop gain (v_O/v_I) of the circuit shown in Fig.Q.7(c)(i). Using this circuit design an inverting amplifier with a gain of 100, input resistance of 1MΩ. For practical reasons, not to use the resistors greater than 1MΩ. Compare your design with the circuit shown in Fig.Q.7(c)(ii). **(08 Marks)**

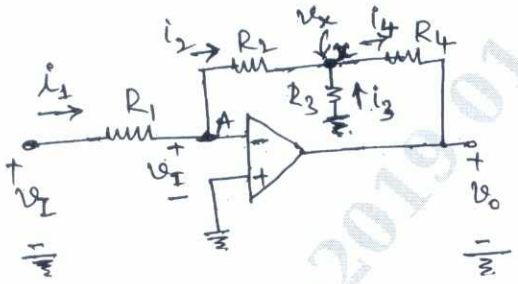

Fig.Q.7(c)(i)

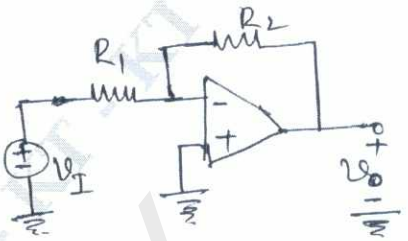

Fig.Q.7(c)(ii)

8 a. Explain the transistor sizing with an example of 4 input NAND gate. **(06 Marks)**

b. Consider a CMOS inverter fabricated in a 0.25μm process for which C_{ox} = 6fF/μm^2, μn C_{ox} = 115μA/v^2, $\mu_p C_{ox}$ = 30μA/v^2, $V_{tn} = -V_{tp}$ = 0.4V, V_{DD} = 2.5V. W/L ratio for Q_N = 0.375 μm/0.25μm and for Q_P = 1.125μm/0.25μm. $C_{gs} = C_{gd}$ = 0.3fF/μm of gate width, C_{dbh} = 1fF, C_{dbp} = 1fF and C_w = 0.2fF. Find t_{PHL}, t_{PLH} and t_P. **(07 Marks)**

c. Explain the parameters used to characterize the operation and performance of logic family. **(07 Marks)**

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10EC64

Sixth Semester B.E. Degree Examination, June/July 2019
Antennas and Propagation

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART - A

1 a. Define the following terms :
i) Beam area ii) Effective height iii) Directivity iv) Radiation pattern. **(12 Marks)**

b. What is Friis formula? How can it be used for the calculation of power at a receiving point. **(05 Marks)**

c. A radio link has 150W transmitter connected to an antenna of $2m^2$ aperture at 2GHz. The receiving antenna has a aperture of $1.5m^2$ and is located at 10km. Find the power delivered to the receiver. **(03 Marks)**

2 a. Define a point source. State the power theorem as applied to a point source. **(06 Marks)**

b. Calculate the directivity of a broad side array of two identical isotropic sources feed with currents of same magnitude and phase spaced $\lambda/4$ apart along the polar axis. The relative field pattern is give by $E = \cos(\pi/2 \cos\theta)$ where θ is the polar angle. **(06 Marks)**

c. Obtain the expression for the field due to a broad side array of n elements. **(08 Marks)**

3 a. Derive the radiation resistances in the case of
i) Thin linear dipole ii) $\lambda/2$ dipole. **(10 Marks)**

b. Given for an antenna $R_r = 73\Omega$, $R_L = 7\Omega$ and G = 10dB. Compute its efficiency and directivity. **(06 Marks)**

c. Write short note on V antennas. **(04 Marks)**

4 a. Derive the expression for the field strengths E_ϕ and H_θ in the case of a small loop. **(10 Marks)**

b. Explain the slot and complementary antennas. **(06 Marks)**

c. Explain microstrip antennas with neat sketches and mention its advantages. **(04 Marks)**

PART - B

5 a. Explain the practical design and operation for the monofilar axial mode helical antenna. **(07 Marks)**

b. Explain the working of log periodic antenna. **(07 Marks)**

c. Explain the theory behind Yagi – Uda array. **(06 Marks)**

6 a. Write short notes on :
i) Antennas for ground penetrating radar.
ii) Ultra – wide band antennas. **(14 Marks)**

b. Explain Turnstile antenna. **(06 Marks)**

7 a. Discuss the different forms of radio wave propagations. **(08 Marks)**

b. Derive an expression for space wave field intensity. **(08 Marks)**

c. A TV transmitter (T) uses an antenna of height 200m. The height of receiving antenna (R) for this transmitter is 20m. Obtain the maximum spacing between T and R through tropospheric propagation. Compute also the radio horizon in this case. **(04 Marks)**

8 a. For Ionospheric layer, derive the expression for conductivity and relative permittivity as a function of electron density and angular frequency. **(08 Marks)**

b. Calculate the value of the operating frequency of the ionospheric layer specified by a refractive index 0.85 and an electron density of 5×10^5 electrons/cm^3. **(04 Marks)**

c. Calculate the value of the skip distance given that the height of the ionospheric layer is 50km, MUF is 29MHz and its critical frequency is 4MHz. **(04 Marks)**

d. Write short note on Diffraction. **(04 Marks)**

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10EC65

Sixth Semester B.E. Degree Examination, June/July 2019
Operating Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART - A

1 a. Define an Operating System. What are the different facts of user convenience? **(06 Marks)**

b. Explain Partition based and pool based resource allocation. **(06 Marks)**

c. Explain time sharing operating system with respect to :
i) Scheduling ii) Memory Management. **(08 Marks)**

2 a. Explain the following :
i) Semantic gap ii) Layered operating system structure. **(08 Marks)**

b. Compare Kernel based and Micro Kernel based OS functions. **(06 Marks)**

c. Explain Virtual Machine Operating System [VMOS] with example. **(06 Marks)**

3 a. In some situations a change in the state of one process may cause a change in the state of another process. Describe all such situations. **(08 Marks)**

b. An application is to be coded using threads. Describe conditions under which you would recommend use of i) Kernel level threads ii) User level threads. **(06 Marks)**

c. Explain the different status of process in UNIX OS with diagram. **(06 Marks)**

4 a. Explain the working of a buddy system allocator. **(06 Marks)**

b. Define Boundary tag. Explain merging of free areas using boundary tags. **(08 Marks)**

c. Compare contiguous and non – contiguous memory allocation. **(06 Marks)**

PART - B

5 a. Consider the page reference string 5, 4, 3, 2, 1, 4, 3, 5, 4, 3, 2, 1, 5. How many page faults would access for the following page replacement policies assuming 3 frames?
i) FIFO ii) LRU. **(08 Marks)**

b. Explain the important concept in the operation of demand paging. **(12 Marks)**

6 a. Explain the organisation of sequential access and direct access files. **(08 Marks)**

b. Describe the interface between file system and IOCS. **(08 Marks)**

c. Describe file system actions during a file operation. **(04 Marks)**

7 a. With diagram explain the working of a long, medium and short term scheduling in a time sharing system. **(10 Marks)**

b. Describe the shortest request next [SRN] and highest response next [HRN] scheduling policies and determine the average turn around time and weighted turn around time for the following set of process shown in the below table. **(10 Marks)**

Processes	P_1	P_2	P_3	P_4	P_5
Arrival time	0	2	3	4	8
Service time	3	3	5	2	3

8 a. What is Mail box? Explain features and advantages. **(08 Marks)**

b. Explain the Primary issues in implementing message passing. **(06 Marks)**

c. Explain the Inter – process communication mechanisms in Unix OS. **(06 Marks)**

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10EE61

Sixth Semester B.E. Degree Examination, June/July 2019

Power System Analysis and Stability

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions, selecting at least TWO questions from each part.***
2. ***Missing data, if any, may be suitably assumed.***

PART – A

1 a. For the given one line diagram shown in Fig.Q1(a), draw impedance diagram and reactance diagram.

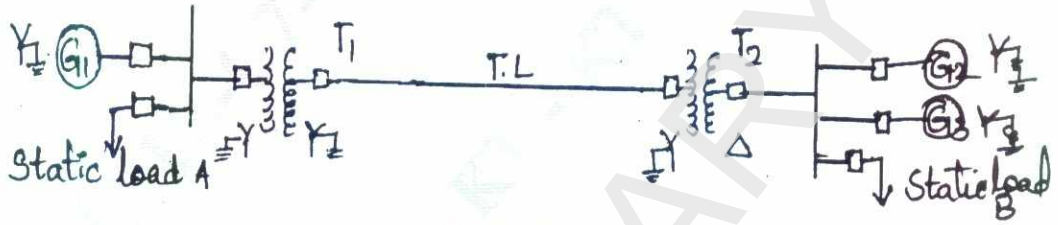

Fig.Q1(a) **(05 Marks)**

b. List any five advantages of PU system. **(05 Marks)**

c. The one line diagram of an unloaded power system is shown in Fig.Q1(c). Reactances of the 2 sections of the transmission line are shown on the diagram. The generator and transformer are rated as follows:
Gen 1 : 20 MVA, 13.8 KV, X″ = 0.2 pu
Gen 2 : 30 MVA, 18 KV, X″ = 0.2 pu
Gen 3 : 30 MVA, 20 KV, X″ = 0.2 pu
Tr : T_1 : 25 MVA, 220 KV/13.8, X″ = 0.1 pu
Tr : T_2 : 1-ϕ units each rated 10 MVA, 127/18 KV, X = 10%
Tr : T_3 : 35 MVA, 220 Y/22Y KV, X = 10%.
Draw the impedance diagram with all reactances marked in pu. Choose a base of 50 MVA, 13.8 KV.

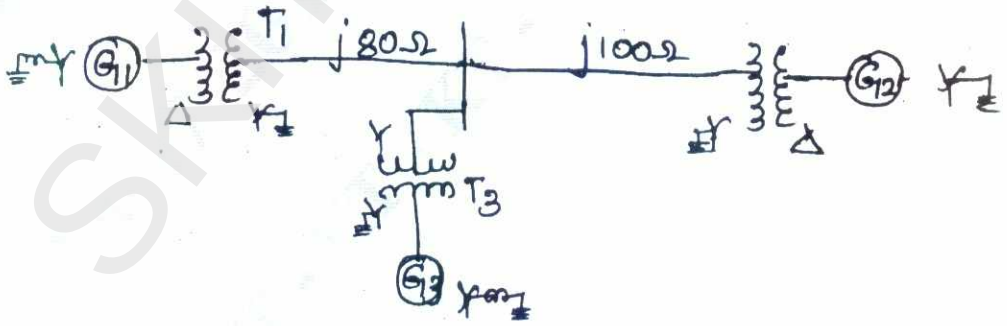

Fig.Q1(c) **(10 Marks)**

2 a. Draw the oscillogram of the short circuit current of a synchronous machine and obtain the expressions for X_d, X'_d, X''_d with the help of suitable equivalent circuits and hence show that $X''_d < X'_d < X_d$. **(10 Marks)**

b. Two generators are connected in parallel to the L.V. side of 3-ϕ Δ-Y transformer as shown in Fig.Q2(b). Ratings of Gen.1 is 50,000 KVA, 13.8 KV and that of Gen 2 is 25000 KVA, 13.8 KV and each generator has subtransientiial reactance of 25%. The transformer is rated 75000 KVA, 13.8 Δ-69YKv, with a reactance of 10%. Before the fault occurs, the voltage on the H.T. tr: is 66 KV. The tr: is unloaded and there is no circulating current between the generator. Find the subtransientiial current in each gen in pu, when a 3-ϕ S.C occurs on the H.T. side of tr:. Select a base in H.T. circuit.

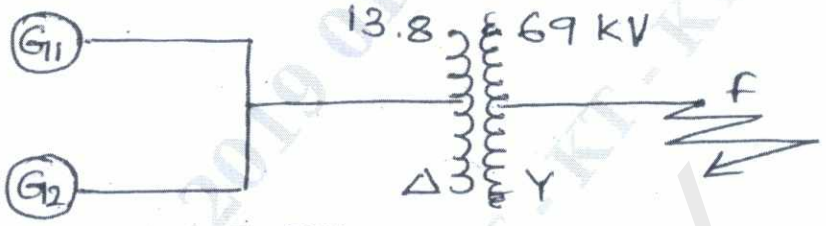

Fig.Q2(b) **(10 Marks)**

3 a. Prove that a balanced set of 3-ϕ voltages will have only positive sequence components of voltages. **(06 Marks)**

b. One conductor of a 3-ϕ line is open. The current flowing to the Δ-connected load through line 'a' is 10A. With the current in line 'a' as reference and assuming that line 's' is open, find the symmetrical components of the line currents. **(07 Marks)**

c. Obtain the relation between sequence components of phase and line currents in delta connected systems. **(07 Marks)**

4 a. For the following configurations of a 3-ϕ transformer, draw the winding connection and zero sequence network. **(08 Marks)**

i) Y - Δ ii) Δ - Δ iii) Y - Y iv) Y - Δ

b. In a 3-ϕ, 4 wire system, the sequence voltages and currents are,

$V_{a_1} = 0.9\angle 10^\circ$ pu; $V_{a_2} = 0.25\angle 110^\circ$ pu; $V_{a_0} = 0.12\angle 300^\circ$ pu

$I_{a_1} = 0.75\angle 25^\circ$ pu; $I_{a_2} = 0.15\angle 170^\circ$ pu; $I_{a_0} = 0.1\angle 330^\circ$ pu

Find the complex power in pu. If the neutral gets disconnected, find the new power. **(08 Marks)**

c. Draw a zero sequence network for the given one line diagram shown in Fig.Q4(c).

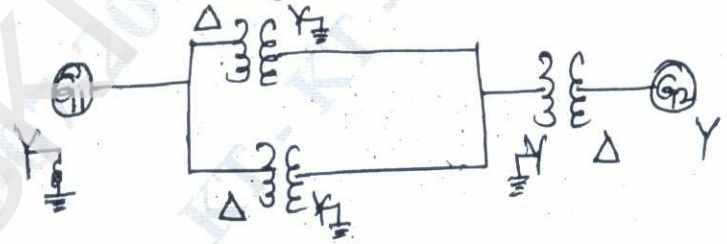

Fig.Q4(c) **(04 Marks)**

PART – B

5 a. Show that, the fault current in an unloaded generator is zero, if the neutral is not grounded in the case of LLG fault, with suitable circuit diagram and sequence networks, after deriving the expression for fault current. **(10 Marks)**

b. A 3-ϕ generator with line to line voltages of 400 V is subjected to an LLG fault. If $Z_1 = j2\Omega$, $Z_2 = j0.5\Omega$ and $Z_0 = j0.25\Omega$, determine the fault current and terminal voltages. **(10 Marks)**